



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/529,990

03/31/2005

Ralf Brederlow

10808/228

5401

48581

7590

09/06/2006

BRINKS HOFER GILSON & LIONE
INFINEON
PO BOX 10395
CHICAGO, IL 60610

EXAMINER

LE, THAO P

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

81

Office Action Summary	Application No. 10/529,990	Applicant(s) BREDERLOW ET AL.	
	Examiner Thao P. Le	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 7/11/06.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicant's arguments, see remarks, filed 07/11/2006, with respect to the rejection(s) of claim(s) 1-9, 11 under 102(b) and claim 10 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made.

Claims 1, 3 are amended and claim 19 is newly added.

Claims 1-11 and 19 are pending.

Claim Rejections

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 11, 19 are rejected under 35 USC 102 (b) as being anticipated by Takemura et al., U.S. Patent No. 6,160,269.

Regarding claim 1, Takemura discloses an IC arrangement,
having an electrically insulating region (lines 24-26, Col. 10, Fig. 3A),

a capacitor (lines 60-64, Col. 11) which contain, in order specified:

An electrode region 307 near the insulating region (the electrode region 203 formed on the insulating region);

A dielectric region 301;

An electrode region 314 remote from the insulating region, the insulating region being part of the insulating layer arranged in a plane (See Figs. 3A-3C);

the capacitor and at least one active component of the IC (the active component is the MOS transistor in Figs. 3A-3F) arrangement being arranged on the same side of the insulating layer and the electrode region 307 near the insulating region and an active region being arranged in a plane with lies parallel to the plane in which the insulating layer is arranged (Figs. 3E-3F);

wherein the electrode region 307 near the insulating region is a monocrystalline region (a-si layer is crystallized to become single-crystal; lines 28-29, Col. 10; lines 4-12, Col. 11; related art: lines 25-40, Col. 1) containing a multiplicity of webs (the webs are transistors that covered by layer 315, Fig. 3D).

Regarding claim 2, Takemura discloses the active component is a transistor (the MOS transistors formed on left side of Figs. 3D-3F).

Regarding claim 3, Takemura discloses the electrode region 314 remote from the insulating region comprises metal-simiconductor compounds (the gate electrode region 314 includes metal and insulating layer made of AlO, same as gate 208 and semiconductor layer 217 of Fig. 2D, lines 40-42, Col. 9).

Regarding claim 4, Takemura discloses the electrode region near the insulating region contains a multiplicity of webs whose web height is larger than the web width (transistor regions, Fig. 3F).

Regarding claim 5, Takemura discloses the control electrode (formed by metal, conductive) has different material than the dielectric layer (formed by dielectric material).

Regarding claims 6, 19, Takemura discloses the electrode region 314 remote from the insulating region adjoins metal-semiconductor compounds (the gate electrode region 314 includes metal and metal semiconductor layer is AIO, same as gate 208 and semiconductor layer 217 of Fig. 2D, lines 40-42, Col. 9).

Regarding claim 7, Takemura discloses one terminal region or both terminal regions (source, drain) of the transistor adjoin the insulating layer (Fig. 3E, 317, 319).

Regarding claim 8, Takemura discloses the spacers arranged on both sides of the control electrodes 314 and have different material than the electrode layer (the AIO layer formed on the metal control electrode 314, Fig. 3D).

Regarding claim 9, Takemura discloses a terminal region of the transistor adjoins a region containing a metal-semiconductor compound (channel or connecting region, 318, 320, or 322).

Regarding claim 11, Takemura discloses the memory cell contains a capacitor and a transistor or more than one transistor (See Figs. 3E-3F).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura et al., U.S. Patent No. 6,160,269.

Regarding claim 10, it is well known in the art that the selection of the parameters such as energy, concentration, temperature, time, molar fraction, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in energy, concentration, temperature, time, molar fraction, depth, thickness, etc., or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is

not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Imscher* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

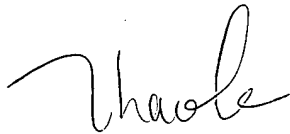
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2818

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thao P. Le', with a stylized, cursive script.

Thao P. Le
Primary Examiner
Art Unit 2818
August 22, 2006.